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SFDR Improvement Algorithms for Current-Steering DACs

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Abstract This paper presents spurious free dynamic range (SFDR) improvement algorithms for current steering digital-to-analog converters (DACs) – targeted for communication applications - taking care of both current source mismatches and glitches. Conventional segmented current steering DAC suffers from static current source mismatches which cause nonlinearity and degrade SFDR, even though glitch energy is suppressed. On the other hand, the conventional data weighted averaging (DWA) algorithm can reduce the static current source mismatch effects, but the glitch energy becomes large which degrades SFDR. In order to suppress both effects, a conventional Switching-Sequence Post-Adjustment (SSPA) calibration and One–Element-Shifting (OES) methods are used as comparison. For further improvement, our investigated algorithms (which are full digital) can suppress the static current source mismatch effects with minimum increase of the glitch energy. By combining these two existed compensation methods, the simulation has been done. Our MATLAB simulation shows that the combination algorithms achieve some improvement in term of SFDR performance by 24 dB, 22dB and 2dB compared to conventional thermometer-coded, one-element-shifting and SSPA method respectively. In case of taking account into current mismatches, this algorithm obtained with 0.02 to 0.2 % higher glitch energy at mismatch switching compared to other 3 methods.

Keyword Current-steering DAC, SFDR, Glitch, Mismatch, Data-Weighted Averaging Algorithm

1. Introduction

Wireless communication systems require high-resolution and high-speed digital-to-analog converters (DACs) with high spurious free dynamic range (SFDR) [1,2], and there in many cases the current steering DAC architecture with combination of the segmented structure for higher bits and the binary weighted structure for lower bits is employed. We have to take into account the static current source mismatches among current sources in the segment structure for higher bits and the glitch energy due to switching timing mismatch to obtain high SFDR performance.

In this paper we investigate algorithms of current source selection in the segmented part so that high SFDR can be achieved; the effects of the current mismatches are reduced and the number of toggling the current switches is small for glitch energy reduction. The algorithms are performed in digital domain, which matches to the VLSI technology advance trend. Our MATLAB simulation shows that the investigated algorithms achieve better SFDR result compared to conventional thermometer method (in case that the static current source mismatches are considered), with 0.2%, 0.02% and 0.2% higher glitch energy at mismatch switching compared to the conventional thermometer-coded, one-element-shifting (OES)[3] and switching-sequence post-adjustment (SSPA)[4] methods respectively.

This paper consists of six sections. Section 2 describes the binary-weighted and segmented - as well as their combination - current steering DAC architectures. Section 3 explains the nonlinearity output due to current source mismatches and glitch effects. Section 4 discusses current-steering DAC configuration algorithm compared with thermometer -coded, OES, SSPA calibration and investigated algorithm. Section 5 discusses measurement results and the conclusion is provided in Section 6.

2. Current steering DAC architecture

A simple current-steering DAC uses binary weighted architecture (Fig.1), where current source values are binary-weighted ($I_1 = I$ $I_2 = 2I$ $I_3 = 4I$). When the digital input is 4, then SW3 turn on and SW1, SW2 turns off, and the current 4I ($=I_3$) flows into the resistor R and the output voltage V_{out} of 4IR is produced. The binary weighted current-steering DAC has advantages of high speed sampling operation, low power and small chip area. However, its disadvantages are that the glitch energy is large and the input-output monotonicity characteristics are not guaranteed.

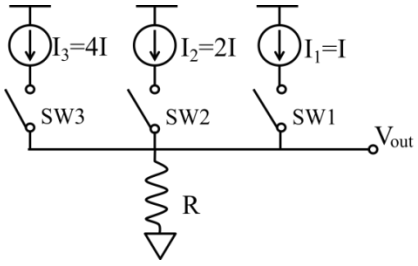


Fig. 1. A 3-bit binary weighted current-steering DAC.

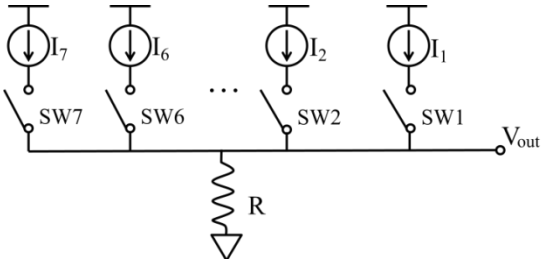


Fig. 2. A 3-bit segmented current-steering DAC.

Segmented architecture of the current-steering DAC is introduced to overcome the binary-weighted disadvantages (Fig. 2). This architecture offers low glitch power energy because 2^N-1 unit current sources with identical weight is used for N-bit resolution, in order to obtain output optimization and flexibility of current source selection as shown in Fig. 2. (Ideally in Fig. 2)

$$I_1 = I_2 = I_3 = I_4 = I_5 = I_6 = I_7 = I \quad (1)$$

When the digital input is 4, then SW1, SW2, SW3, SW4 turn on and SW5, SW6, SW7 turn off, and the current 4I ($=I_1+I_2+I_3+I_4$) flows through the resistor R and the output voltage V_{out} is 4IR. This architecture has advantages that the glitch energy is small and also the input-output monotonicity characteristics are guaranteed, while it has drawbacks of large chip area as well as certain amounts of power increase and sampling speed decrease.

In many cases, their combination is used; for higher bits, the segmented structure is used while for lower bits the binary weighted structure is used. This combined topology can achieve well-balance of chip area [5,6], power, speed and glitch energy [7].

In this paper we assume the combined architecture, but for SFDR improvement, the segmented part for the higher bits is more important and hence our discussion here focuses on the segmented structure.

3. Current-steering DAC non-linearity

Static non-linearity of the current-steering DAC is caused by current source mismatches, while dynamic performance, SFDR, is degraded due to glitch effects [8] as well as current source mismatches.

3.1 Current Source Mismatch

The current source mismatches are inevitable inside an actual chip due to current leakage or imperfect fabrication. Ideally all currents I_1 - I_7 are the same in Fig. 2 as shown in eq. (1), however in reality there are current source mismatches and we define as follows:

$$I = (I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7) / 7 \quad (2)$$

$$I_k = I + dI_k \qquad (k = 1, 2, .. , 7) \quad (3)$$

I is the average current, and dI_k is the deviation of the k-th current source I_k from I. It follows from (2), (3) that

$$dI_1 + dI_2 + dI_3 + dI_4 + dI_5 + dI_6 + dI_7 = 0. \quad (4)$$

These current source mismatches cause the nonlinearity of the current-steering DAC.

3.2 Glitch

Glitch is caused when some current sources turn on and other current sources turn off simultaneously with timing mismatch for digital input change. This glitch effect is severe for the binary-weighted current steering DAC architecture (Fig. 3).

Fig. 3(a)-(d) illustrates an example of glitch effect during mid-code transition in a 4-bit binary-weighted DAC. B0-B3 are switches used to control the current flow of current sources with different weights. These examples demonstrate 0 to 15 possible digital inputs with 7 and 8 as a mid-code for Most Significant Bit (MSB).

Fig. 3(a) shows switch configuration in case that the digital input is 7 (0111). The switch configuration changes simultaneously as the digital input changes from 7 (0111) to 8 (1000). During this transition, the switch configuration has possibility to change either to 0 (0000) or 15 (1111). The transitions in Fig. 3(b) and Fig. 3(c) depend on how fast switch B3 is triggered to the desired input.

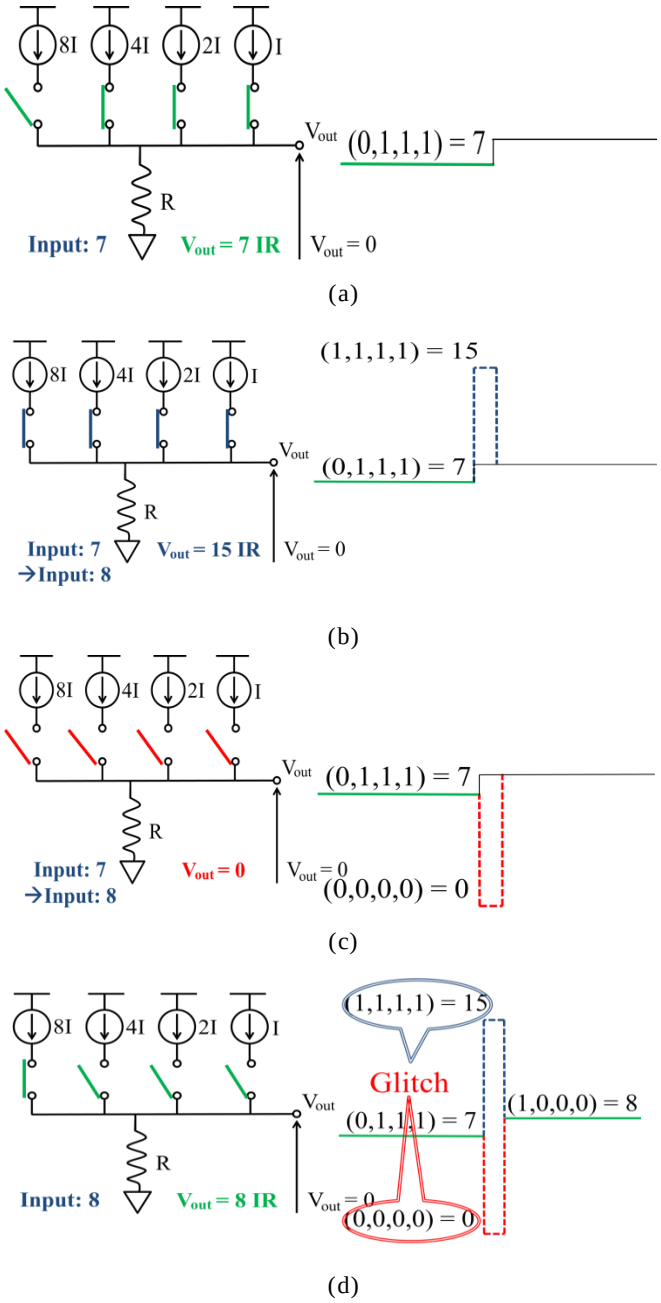


Fig. 3. Explanation of the glitch problem due to timing skew among switch control signals for the current sources in a binary-weighted current-steering DAC.

Fig. 3(d) shows that desired input of 8 (1000) is obtained through transition of input 7 (0111). The produced glitch during transition will affect adversely dynamic performance. The glitch area in sampling period increases with the sampling frequency.

On the other hand, the segmented architecture offers a good solution to reduce glitch [7,8]. For digital input increase, some current switches turn on and no current switches turn off, while for digital input decrease, some current switches turn off and no current switches turn on, and hence glitch energy is small.

4. Current-steering DAC algorithm

The DWA algorithm is introduced mainly in multi-bit Delta-Sigma AD/DA modulators [9,10,11], in order to spread the current source mismatches in the segmented DAC in frequency domain (rigorously speaking, they are noise-shaped), by optimizing the current source selection with the controlled digital input.

However, the DWA algorithm suffers from high glitch effect because all of on-switches turn off and some off-switches turn on in each sampling period. For example, in Fig. 2 suppose that the digital input is 2, then SW1, SW2 turn on and the other switches are off. Next the digital input is 3. Then SW1, SW2 turn off and SW3, SW4, SW5 turn on while SW6, SW7 remain off.

Then we investigate a modified DWA algorithm [12, 13] to spread out the current source mismatch effects in frequency domain while maintaining low glitch effect. The investigated algorithm may be discussed elsewhere (in Delta-Sigma ADC/DAC fields) for static current source mismatch spread spectrum and its easy implementation. However, to our knowledge, the discussion in viewpoint of both current source mismatch spread spectrum and glitch reduction for Nyquist DAC SFDR improvement is new.

4.1 Thermometer Coded (TC) Algorithm

Thermometer coded (TC) algorithm is commonly used for element selection in the segmented current-steering DAC. For the digital input, Din, the elements U1, U2,.. U_{Din} are selected (SW1, SW2,…,SW_{Din} are on, and the others are off).

Fig. 4 shows a 3-bit conventional thermometer coded DAC with setting digital inputs. U1 to U7 represent available initial point and end point current sources in blue and red cells.

(i) When the digital input is 5, current source switches of U1 to U5 turn ON and U6, U7 are off.

(ii) While digital input is 7, U1 .. U5 remain ON, and U6 and U7 are added as ON to the previous output of 5.

(iii) Now suppose that the present digital input decrease to 4. Then U1 to U4 remains ON while U5 to U7 will be turned OFF.

The current source switching configuration continues until all possible inputs tested until output pattern of distortion and mismatch is formed.

Fig. 5 shows DAC output spectrum of current-steering DAC without and with the mismatch, and we see large components in current source mismatch case.

Input	U1	U2	U3	U4	U5	U6	U7	Idx.1 (Start)		Idx.2 (End)
Input: 5								1	-	5
Input: 7								1	-	7
Input: 4								1	-	4
Input: 6								1	-	6
Input: 2								1	-	2
Input: 0								-	-	-
Input: 3								1	-	3
Input: 1								1	-	1

Fig. 4 Current source cell selection with the conventional thermometer coded algorithm.

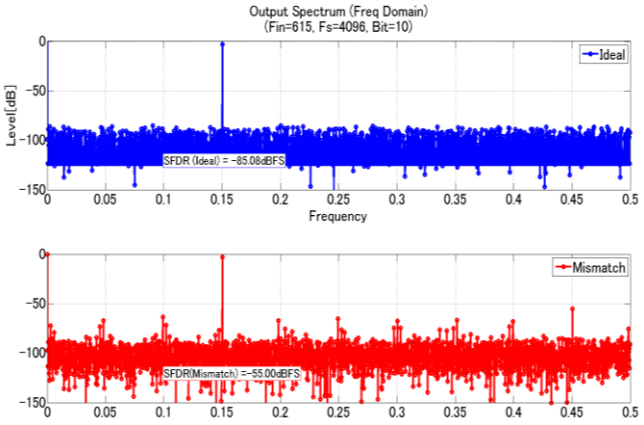


Fig. 5. Simulated output power spectrum of a 10-bit segmented DAC with the conventional thermometer coded algorithm. (a) Without current source mismatch. (b) With current source mismatch.

4.2 One-Element-Shifting (OES) Algorithm

In [3], One-Element-Shifting (OES) is proposed, so that the current mismatch errors are spread out in frequency domain and glitch energy is minimized with decreased number of switching activities.

Fig. 6 explains their operation.

(i) The digital input is 5, U1 to U5 switches are selected to be turned ON while U6 and U7 is OFF.

(ii) When digital input change to 7, U2 to U7 and U1 are selected due to changes of starting point form U1 to U2, shifted by 1 for every clock.

(iii) When digital input is 4, U3 to U6 are selected. Same as in (ii) where the starting points changes from U2 to U3.

(iv) When it is 6, U4 to U7 and U1 to U2 are selected.

This operation continues.

The number of the switching activities is almost minimum; even though it is slightly larger than that of the thermometer-coded algorithm, its increase becomes negligible as the DAC resolution bits increases.

Input	U1	U2	U3	U4	U5	U6	U7	Index1		Index2
Input: 5								1	1+5-1=5	5
Input: 7								1+delay =2	2+7-7-1=1	1
Input: 4								2+delay =3	3+4-1=6	6
Input: 6								3+delay =4	4+6-7-1=2	2
Input: 2								4+delay =5	5+2-1=6	6
Input: 0								5+delay =6	-	-
Input: 3								6+delay =7	7+3-7-1=6	2
Input: 1								7+delay =8-7=1	1+1-1=1	1

Fig. 6. Current source cell selection for One Element Shifting (OES).

4.3 Switching Sequence Post Adjustment (SSPA) Algorithm

The SSPA calibration method is a method that can changes the switching sequence of current sources especially after fabrication process. It is a simple calibration method which only requires a current comparator to find out the best arrangement of current sources. By implementing this calibration method, the best Integral Non-Linearity (INL) of a DAC can be obtained. At the same time, it will contribute on SFDR improvement. In [4], the extra current source dummies are used in order to increase the selection if there any defect during the fabrication.

Fig. 7 shows the operational of SSPA calibration method.

(i) The random current sources are compared and sorted from lowest to highest order.

(ii) Then, the sorted current sources are rearranged by arranging small currents between two large currents as in (2).

(iii) After that, each two neighboring currents are summed.

(iv) Then summed currents are again compared, sorted and rearranged as in (i) and (ii).

(v) Finally, the final sequence is obtained.

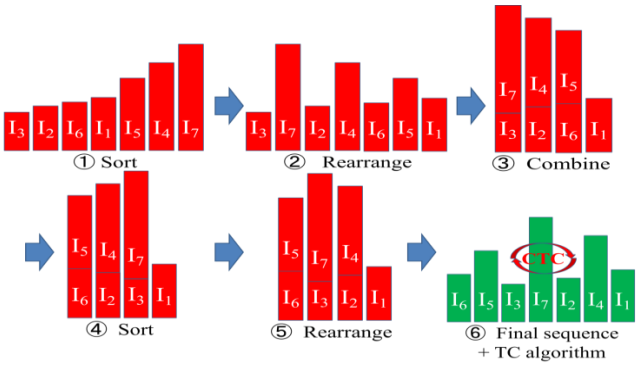


Fig. 7. Steps of SPPA calibration

4.3 Investigated Algorithm

Our investigated algorithm is combination of SSPA and OES algorithms. In order to suppress more current mismatch errors into the noise floor for obtaining a better SFDR performance. Basically, the operation of this method is by implementing SSPA method from step (i) – (v), as explained in chapter 4.2, the difference is we change the method of using thermometer-coded to OES method as shown in Fig. 8. By expecting the conventional SSPA has suffers to glitch and using OES can further reduce the glitch effect even the number of switching is slightly increased.

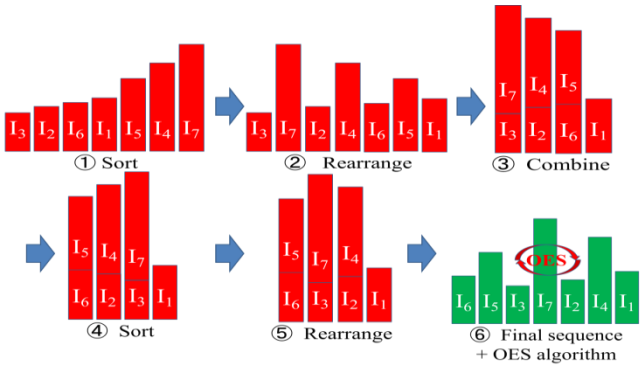


Fig. 8. Investigated algorithm.

5. Simulation result

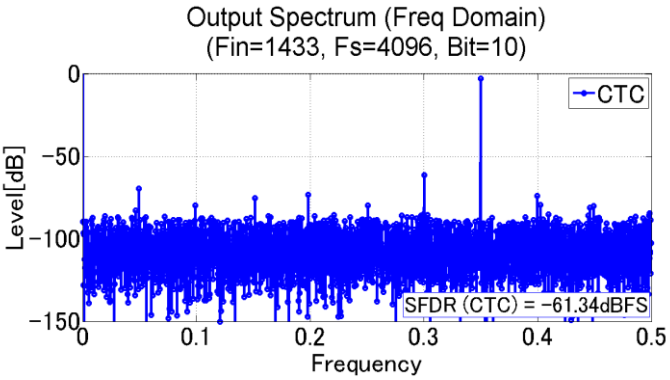
We have implemented the developed algorithms to demonstrate 3 to 10-bit segmented current-steering DACs at 205Hz to 2045 Hz input frequency with 205Hz (0.05fs) step using Matlab simulation. Fig. 9 show one of the simulation results in conditions as summarized in Table 1.

The simulation results show that as the number of bits (DAC resolution) increases, the SFDR average performance improves proportionally. Fig. 9(a)-(d) shows comparison of SFDR performance of a 10-bit current-steering DAC with four difference algorithms, where only current source mismatches are considered and glitch effects are NOT. These algorithms are presented in blue, red, magenta and green lines on the graph. The observation shows that the proposed algorithm obtains 85.37dBFS at condition of frequency input 1433Hz with 6% standard deviation error and 40% mismatch (0.8 to 1.2A) ; 24 dB better SFDR performance compared to the thermometer coded algorithm, 22dB compared to OES algorithm and 2 dB compared to the SSPA algorithm.

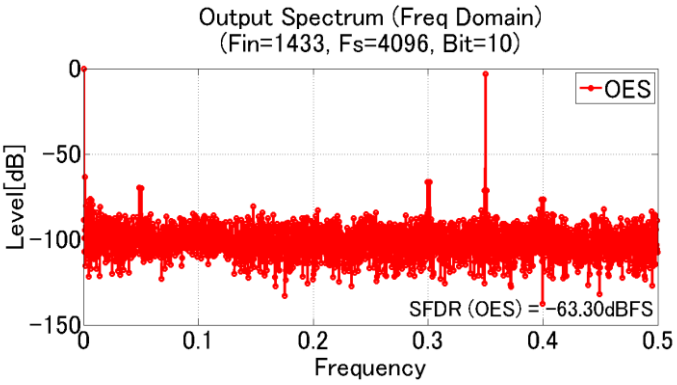
Table 2 shows the summarized SFDR performance of 4 different simulated algorithms and their number of the switching activities. From the results, we see that the investigated algorithm is comparable to the thermometer coded and SSPA and equally with OES due to the based algorithm used. Hence the glitch is expected to be small than the SSPA algorithm due to implementation of OES besides of conventional SSPA.

Table1. Simulation conditions

Input signal		Error	
Input frequency, fin	205 - 2045Hz	Number of errors value	1023
Sampling frequency, fs	4096 Hz	Standard deviation (%)	1 - 6
FFT point	4096	Mismatch (%)	10 - 40



(a)



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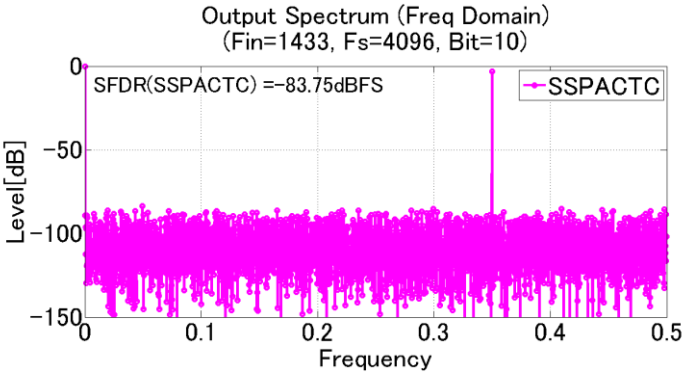
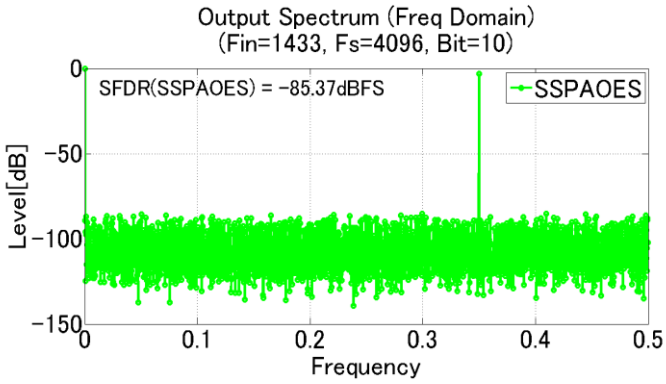


(c)



(d)

Fig. 9. Simulated output power spectrum of an 10-bit current steering DAC using 4 different algorithms. (a) CTC. (b) OES. (c) SSPA-CTC. (d) Investigated algorithm.

Table2. Summary of SFDR comparison for several current cell selection algorithms.

Algorithm	SFDR (dBFs)	SFDR (dBc)	Diff (dB)	Switching Occurrences	Diff (%)
CTC	61.34	58.34	-	2376311	-
OES [3]	63.30	60.29	+1.96	2380181	+ 0.16
SSPACTC [4]	83.75	80.73	+22.41	2376311	0.0
Investigated	85.37	82.37	+24.03	2380692	+ 0.18

6. Conclusion

This paper has investigated SFDR improvement algorithms of the current-steering DAC with taking care of current source mismatches and glitch. We have validated our methods with Matlab simulation. Extending our methods to more complicated algorithms are relatively easy because our algorithms are fully digital which matches to the VLSI technology advance trend.

We close this paper by remarking that conventional SSPA in [4] uses a current comparator with sophisticated analog circuit design, however a time-domain analog method of digital circuit implementation for current comparison in [14] would make the investigated method more practical in fine CMOS process.

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